Analysis of Aluminum-Nitride SOI for High-Temperature Electronics

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Outline

• Background (why and what)
• Simulation Results
  • Leakage Current (OFF)
  • Subthreshold (OFF to ON)
  • High Current (ON)
• Conclusions
NASA Interest in High-Temp Electronics

Spacecraft electronics temperature-sensitive:
- face hot and cold extremes
- constant thermal management required

Future: sensors, comm during atmospheric entry
Earth orbit: 100K to 400K

Black-Body Sphere Temperature in Solar Orbit

\[ T = \frac{279K}{\sqrt{D}} \]
Focus of This Work

Electronics Technology (NASA application):
- Near-term ⇒ silicon-based CMOS
- Rad-hard ⇒ silicon-on-insulator (SOI)
- Minimize self-heating ⇒ Aluminum-Nitride insulator (high thermal cond.)
- High integration, low power ⇒ small
- High temp. operation ⇒ up to 500K

Simulation Technology:
- Thermal effects ⇒ electrothermal model
- Easily modifiable model ⇒ PDE solver (PROPHET)

Exploratory attempt to use a PDE solver for AlN-based SOI electrothermal simulation
Devices Simulated

a) Bulk MOSFET

- Source
- Gate
- Drain
- n-Si
- Current
- p-Silicon substrate

κ = 145 W/m·K
κ = 1.45 W/m·K

b) SiO₂ SOI MOSFET

- Source
- Gate
- Drain
- n-Si
- Cur. Heat
- p-Silicon substrate

SiO₂
κ = 1.4 W/m·K
κ = 1.45 W/m·K

κ = 136 W/m·K
κ = 1.45 W/m·K

Doping (Large & Small)

Epitaxial-Si: 1e17 p-type
Si Substrate: 5e15 p-type
Poly-Si Gate: 1e20 n-type
Source/Drain: 1e20 n-type

Large: L=2.50μm, D(Si)=0.20μm, D(Ins)=0.6μm, D(ox)=10nm
Small: L=0.25μm, D(Si)=0.05μm, D(Ins)=0.2μm, D(ox)=4nm
Simulation region size: 5μm x 5μm
Main thermal contact: Back
Substrate: κ = 0.01κ(Si) (~500 μm substrate)
Thermal contact at Source/Drain:
- approximate thermal transfer to top-side
Electrothermal Model

Electrothermal Model (self-consistent charge and heat transport):

\[ \nabla \cdot (\varepsilon \nabla \psi) = -q(p - n + N) \]

\[ \frac{\partial n}{\partial t} = \nabla \cdot [D_n \nabla n - n \mu_n \nabla \psi] - R \]

\[ \frac{\partial p}{\partial t} = \nabla \cdot [D_p \nabla p + p \mu_p \nabla \psi] - R \]

\[ C_L \frac{\partial T_L}{\partial t} = \nabla \cdot (\kappa \nabla T_L) + J \cdot E \]

Solution variables:
- potential, \( \psi \)
- electron density, \( n \)
- hole density, \( p \)
- lattice temp, \( T_L \)

Temperature-dependence included:
- \( D_n, D_p, \mu_n, \mu_p, \kappa, n_i, N_C, N_V, E_G \)

Assumptions in this work:
- steady-state; \( T_{env} = 300K, 400K, 500K \)
- Maxwell-Boltzmann statistics (little change with Fermi-Dirac)
Drain Leakage Current Simulation

Ramp $V_D$ at $V_G = 0$V (nominal OFF)
Large ($L = 2.50 \mu$m) MOSFETs: $0 \leq V_D \leq 10$
Small ($L = 0.25 \mu$m) MOSFETs: $0 \leq V_D \leq 3$

**Expectations:**
- No self-heating (low current): SiO$_2$ and AlN SOI same
- MOS: Higher leakage (junction EHP generation); worse at high T
Expectations met: Bulk MOS has higher leakage; SiO$_2$ & AlN SOI same
Surprise: these short-channel SOIs have higher leakage, and differ...
Drain Leakage - Small MOSFET Detail

2-D Electrostatic Potential (300K, $V_D=3$)

- **0.25 µm** Bulk MOS
- **0.25 µm** AlN SOI
- **S** and **D** represent Source and Drain, respectively
- **Si** and **AIN** layers
- **Electron Barrier**

Small SOI devices fully-depleted: DIBL \(\Rightarrow\) higher OFF current
Ramp $V_G$ at $V_D = 0.1V$ (turn-ON characteristic)

Large ($L = 2.50 \mu m$) MOSFETs: $0 \leq V_G \leq 10$

Small ($L = 0.25 \mu m$) MOSFETs: $0 \leq V_G \leq 3$

**Expectations:**

- No self-heating (low $V_D$): SiO$_2$ and AlN SOI same
- Large PD SOI: same as Bulk MOSFET (inversion layer in epi-Si)
- Small FD SOI: unknown...
Subthreshold Current - Large MOSFETs

Expectations met: Devices virtually identical in subthreshold

(STS: Subthreshold Slope)

- Bulk SiO₂
- AlN

(V_D=0.1V)

Gate Voltage, V_G (V)

Drain Current, I_D (mA/µm)

80mV/decade

112mV/decade

154mV/decade

400K

300K

500K
Subthreshold Current - Small MOSFETs

Surprise: SiO\(_2\) SOI better STS than Bulk MOS; AlN SOI slightly worse

Drain Current, \(I_D\) (mA/\(\mu\)m) vs. Gate Voltage, \(V_G\) (V)

- Bulk SiO\(_2\)
- SiO\(_2\)
- AlN

Temperature:
- 300K: 70±3 mV/dec
- 400K: 98±5 mV/dec
- 500K: 130±7 mV/dec

\((V_D=0.1V)\)
SiO$_2$ SOI has $\Delta n$ in epi-SI; AlN SOI has significant $\Delta n$ in substrate
High-Current (Device ON) Simulation

Ramp $V_D$ at $V_G = 3V$ (ON characteristic)
Long Channel ($L = 2.5 \, \mu m$) devices: $0 \leq V_D \leq 10$
Short Channel ($L = 250 \, nm$) devices: $0 \leq V_D \leq 3$

Expectations:
- Significant self-heating (high current and high $V_D$)
- SiO$_2$ SOI: significantly reduced current drive
- AlN SOI and Bulk MOS: similar self-heating
High Current - Large MOSFETs

Self-heating significantly degrades SiO$_2$ SOI current; AlN SOI mitigates
High Current - Small MOSFETs

SiO$_2$ SOI self-heating effects (current decrease, NDC) increase with $T_{env}$
Carrier mobility degrades with temperature (self-heating and $T_{\text{env}}$).
Temperature & Self-Heating - Large MOSFETs

**2-D Temperature Plot (T\textsubscript{env} = 500K)**

- **SiO\textsubscript{2}**-based SOI will melt itself at 500K T\textsubscript{env}
- AlN SOI dramatically mitigates self-heating

**Summary:**

- SiO\textsubscript{2}-based SOI will melt itself at 500K T\textsubscript{env}
- AlN SOI dramatically mitigates self-heating
Conclusions

Conclusions

• AlN eliminates self-heating penalty of SOI $\Rightarrow$ high-T silicon SOI
• PDE-solver device modeling works, even for electrothermal model
• Careful design of FD SOI required to optimize leakage, subthreshold
• High $\kappa$ of AlN allows thick SOI insulator - new design flexibility

Future Work:

• optimize SOI device structure
• add impact ionization (kink/BJT effect)
• add body contact (minimize floating body effects)
• simulate full CMOS
• add quantum effects for ultra-small device simulation