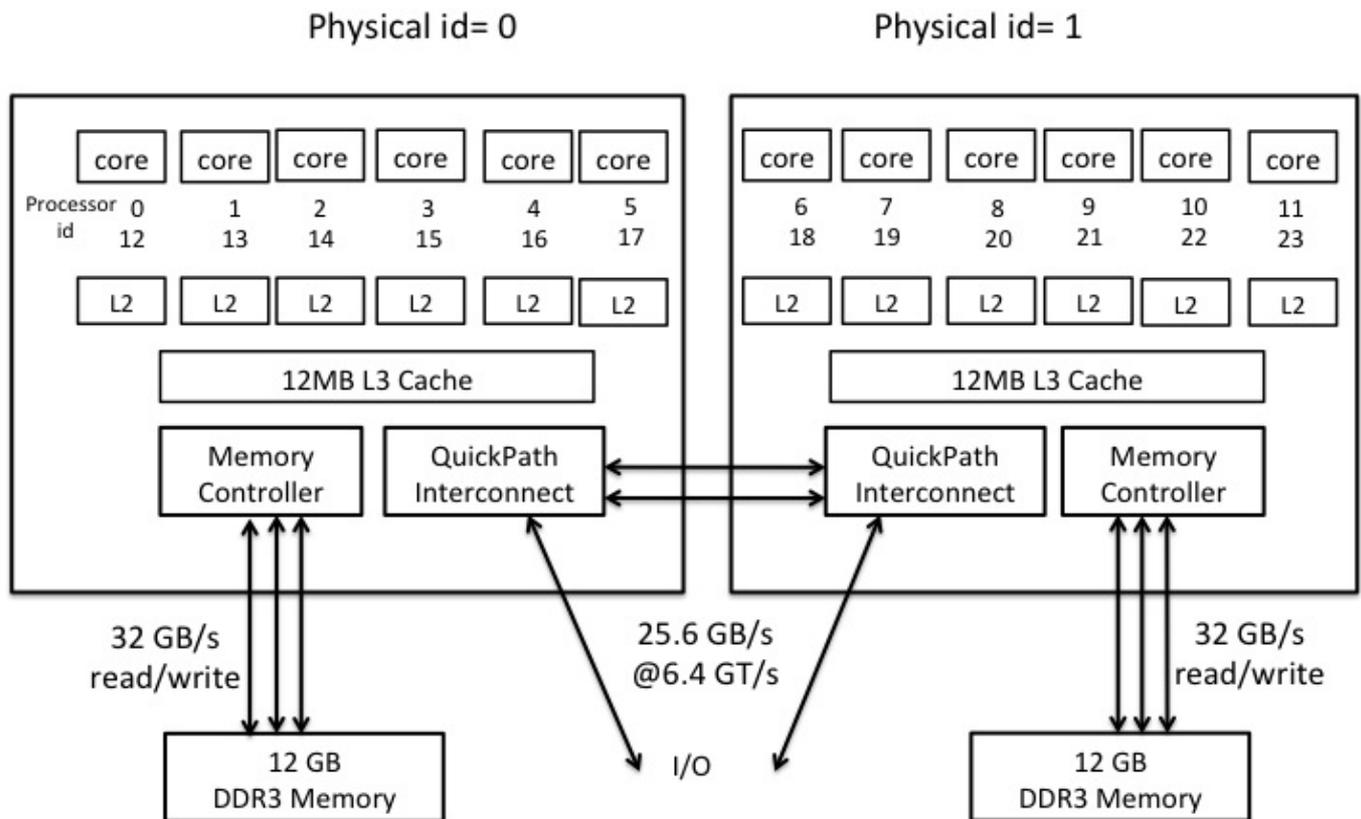


Westmere Processors

Category: Pleiades

Configuration of a Westmere Node



Core Labeling

Unlike Harpertown, the core labeling in Westmere is contiguous. That is, cores 0-5 are in the first socket and cores 6-11 are in the second socket.

When using the SGI MPT library, the environment variable **MPI_DSM_DISTRIBUTE** is set to ON by default for the Westmere nodes.

SSE4 Instruction Set

Intel's Streaming SIMD Extensions 4.2 (SSE4.2) instruction set is included in the Westmere processors.

Since the instruction set is upward compatible, an application that is compiled with `-xSSE4.1` (with Intel version 11 compiler) can run on Harpertown, Nehalem-EP, Westmere, or Sandy Bridge processors. An application that is compiled with `-xSSE4.2` can run only on Nehalem-EP or Westmere processors. An application that is compiled with `-xAVX` can run only on Sandy Bridge processors.

TIP: If you want to have a single executable that will run on any of the four Pleiades processor types, with suitable optimization to be determined at runtime, you can compile your application with `-O3 -ipo -xAVX -xSSE4.1`.

Hyperthreading

Hyperthreading is available by user request on the Westmere nodes (for example, by asking for more than 12 ranks per node).

Turbo Boost

Turbo Boost is set to ON on the Westmere nodes.

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<http://www.nas.nasa.gov/hecc/support/kb/entry/80/?ajax=1>