Pleiades Configuration Details

Category: Pleiades

DRAFT

This article is being reviewed for completeness and technical accuracy.

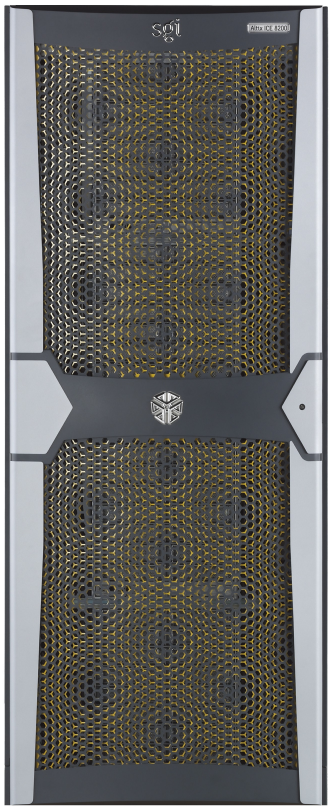
Pleiades Hardware Hierarchy

The hardware hierarchy from a single processor to the whole Pleiades supercluster is described below:

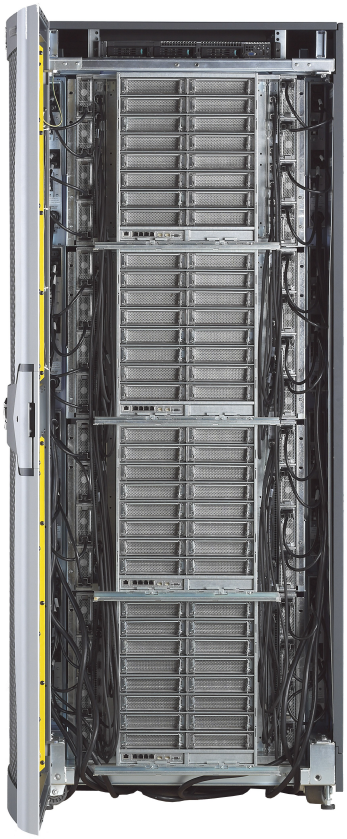
- one quad-core (Harpertown, Nehalem-EP) or 6-core (Westmere) processor per socket
- 2 sockets in 1 node
- 16 compute nodes (labeled as n0 - n15) in 1 IRU (individual rack units)
- 4 IRUs (labeled as i0 - i3) in 1 rack
- 91 Harpertown racks (labeled as r1-r91);
  20 Nehalem-EP racks (labeled as r161-170, r177-186):
  and 73 Westmere racks (labeled as r129-160, r171-176, r187-218, r219, r221-r222)
  in the Pleiades supercluster

The nomenclature of a Pleiades compute node is based on which rack and IRU it is on. For example, r1i0n15 is the node 15 in IRU 0 of rack 1.

Below are the front views of a typical rack:



Front view of a rack



Front-open view of a rack (includes 4 IRUs)

Processor and Memory Subsystems Statistics

Below are detailed configuration statistics for the processor and memory subsystems for all Pleiades nodes:

Pleiades Processor and Memory Subsustems Statistics

Hostname	**pfe[1-12] bridge[1-2]**	**pbspl1, pbspl3**	**r[1-91]i[0-3]n[0-15]**	**r[161-170,177-186] i[0-3]n[0-15]**	**r[129-160,1 219, 221-22 i[0-3]n[0-15**
Function	front-end * bridge node with Columbia CXFS filesystems mounted	PBS server	compute	compute	compute
Architecture	ICE 8200EX	ICE 8200EX	ICE 8200EX	ICE 8200EX	ICE 8400EX
			Processor		
CPU	**Quad-Core Xeon E5472 (Harpertown)**	**Quad-Core Xeon E5472 (Harpertown)**	**Quad-Core Xeon E5472 (Harpertown)**	**Quad-Core Xeon X5570 (Nehalem-EP)**	**6-Core Xeon X567 (r221-222)**

					(Westmere
CPU-Clock	**3.00 GHz**	**3.00 GHz**	**3.00 GHz**	**2.93 GHz**	**2.93/3.06 (r**
Floating Point Operations per cycle per Core	4	4	4	4	4
# of Cores/blade (or node)	8	8	8	8	12
Total # of nodes	.	.	5,824	1,280	4,672
Total # of Cores	.	.	46,592	10,240	56,064
			Memory		
L1 Cache	Local to each core; Instruction cache: 32K Data cache: 32K; 32B/cycle;	Local to each core; Instruction cache: 32K Data cache: 32K; 32B/cycle;	Local to each core; Instruction cache: 32K Data cache: 32K; 32B/cycle;	Local to each core; Instruction cache: 32K Data cache: 32K; 32B/cycle;	Local to eac Instruction c Data cache 32B/cycle;
L2 Cache	12MB on-die for the Quad-Core; 6MB per core pair; shared by the two cores.	12MB on-die for the Quad-Core; 6MB per core pair; shared by the two cores. L2 Cache speed: 3 GHz	12MB on-die for the Quad-Core; 6MB per core pair; shared by the two cores. L2 Cache speed: 3 GHz	256 KB per core	256 KB per
L3 Cache	N/A	N/A	N/A	8 MB shared by the four cores	12 MB shar cores
TLB	local to each core	local to each core	local to each core	local to each core	local to eac
Default Page Size	4 KB	4 KB	4 KB	4 KB	4 KB
Local Memory/Core	**2 GB (pfe[1-12]); 8 GB (bridge[1-2]; Fully Buffered DDR2 DIMM**	**2 GB**	**1 GB**	**3 GB; DDR3**	**2 GB: DDR**
		16 GB	8 GB	24 GB	24 / 48(r21

Total Memory/node	16 GB (pfe[1-12]); 64 GB (bridge[1-2])				
Front-Side Bus	1600 MHz; 25.6 GB/sec read 12.8 GB/sec write	1600 MHz; 25.6 GB/sec read 12.8 GB/sec write	1600 MHz; 25.6 GB/sec read 12.8 GB/sec write	N/A	N/A
Memory Controller	N/A	N/A	N/A	32 GB/sec read/write	32 GB/sec r
QuickPath Interconnect	N/A	N/A	N/A	25.6 GB/sec	25.6 GB/se

One of the Harpertown racks, rack 32, provides 16 GB of memory per node, double the size of per-node memory available in the other Harpertown racks.

Related articles:

Pleiades Hardware Overview

Harpertown Processors

Nehalem-EP Processors

Westmere Processors

Comparison among Harpertown, Nehalem-EP, and Westmere

Pleiades Home Filesystem

Pleiades Lustre Filesystems

Pleiades Front-End Usage Guidelines

Article ID: 77
Last updated: 21 Oct, 2011
Computing at NAS -> Computing Hardware -> Pleiades -> Pleiades Configuration Details
http://www.nas.nasa.gov/hecc/support/kb/entry/77/?ajax=1